REMARKS

This Amendment seeks to place this application in condition for allowance. New claims 176-186 have been added to more fully claim Applicant's invention. Several of the pending claims have been amended. No new matter has been added.

Office Action:

In the office Action mailed March 9, 2001, claims 151-175 were objected to, due to informalities, namely the right margin of pages in the amendment filed Sept 25, 2000 being too small. In addition, claims 151-164, 168 and 170 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Substitute Amendment

To correct the right margin spacing of pages in the amendment filed Sept 25, 2000, Applicants have enclosed herein, under a separate cover sheet "EXHIBIT B", a substitute Preliminary Amendment which complies with 37 CFR 1.52(a). This substitute Preliminary Amendment is an identical version of the Preliminary Amendment filed Sept 25, 2000. No new matter has been added.

Rejection 35 U.S.C. §112:

Claims 151-164, 168 and 170 have been amended to correct typographical errors which arose from the right margin of several pages of the amendment filed Sept 25, 2000 being too small. Amendments to

B

the claims are shown herein in clean form as is now in effect per 37 CFR §1.121. A copy of all of the pending claims, including mark-ups to show deletions and insertions is also attached hereto as EXHIBIT A. No new matter has been added.

INFORMATION DISCLOSURE STATEMENT

In compliance with the duty of disclosure set forth in 37 C.F.R. §1.56, Applicants' submit concurrently herewith an Information Disclosure Statement (IDS) including modified Form PTO-1449. A copy of that IDS and modified Form PTO-1449 are attached hereto.

Documents listed in the PTO-1449 have been cited by a defendant in an action pending in U.S. District Court For Eastern District of Virginia case, namely in Rambus Inc. v. Infineon Technologies A.G., et al., as prior art against the inventions claimed in, among other patents, U.S. 6,032,214. The '214 patent is a grandparent of the instant application. Reference to these documents are listed on page 2 of the Defendents' AMENDED PRIOR ART NOTICE PURSUANT TO 35 U.S.C. §282 (hereinafter 'PRIOR ART NOTICE'). A copy of the PRIOR ART NOTICE is included with the IDS submission.

Furthermore, the construction or interpretation of a number of terms have recently been considered in a *Markman* opinion issued in the above-mentioned litigation. A number of claims pending in the instant application incorporate or incorporated some of these terms including, for example, the terms "block size", "read request", "write request", and "bus". The terms "read request" and "write request" have been deleted from the pending claims (as amended). The term "bus" has been deleted from some of the pending claims (as amended). A discussion of

"block size" may be found on pages 41-47 of the *Markman* opinion, and a discussion of "bus" may be found on pages 17-41 of the *Markman* opinion. By submission of this *Markman* opinion, Applicants make no statement as to the correctness of the constructions set forth therein. Indeed, as is apparent from that opinion, the court substantially adopted the constructions proposed by Infineon, and not that construction proposed by Rambus. A copy of the *Markman* opinion is also enclosed herewith.

CONCLUSION

Applicants request entry of the foregoing amendment prior to examination of this application. Applicants submit that all of the claims present patentable subject matter. Accordingly, Applicants respectfully request allowance of all of the claims.

Respectfully submitted,

Date: April 20, 2001

Neil A. Steinberg
Reg. No. 34,735
650-947-5325

EXHIBIT A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

151. (Amended) A method of controlling a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of controlling the memory device comprises:

issuing a first operation code [a read request] to the memory device, wherein in response to the first operation code, [read request,] the memory device outputs first and second portions of data [onto a bus];

sampling the first portion of data [from the bus] synchronously with respect to a rising edge transition of an external clock signal; and

sampling the second portion of data [from the bus] synchronously with respect to a falling edge transition of the external clock signal.

152. (Amended) The method of claim 151 further including:

providing block size information to the memory device, wherein the block size information defines an amount of data to be output by the memory device [onto a bus in response to the read request;

wherein

a first portion of the amount of data is sampled from the bus synchronously with respect to a rising edge transition of an external clock signal; and

a second portion of the amount of data is sampled from the bus synchronously with respect to a falling edge transition of the external clock signal].

153. (Amended) The method of claim 151[152] wherein, in response to the first operation code [read request], the first portion of [the amount of] data is output [onto the bus] after a programmed amount of time [delay time] transpires.

154. (Amended) The method of claim 151 [153] further including:

providing access time information to the memory device; and

issuing a second operation code, wherein in response to the second operation code, the memory device stores the access time information in a register within the memory device.

155. (Amended) The method of claim 154 wherein the access time information is representative of a number of clock cycles of the external clock signal to transpire before the first portion [of the

amount] of data is output by the memory device [onto the bus] in response to the first operation code.

156. The method of claim 151 wherein both the rising and falling edge transitions of the external clock signal include voltage swings of less than one volt.

157. (Amended) A controller device for controlling a synchronous memory device, the controller device comprising:

output driver circuitry to [output] provide an operation code [a read request] to the memory device, wherein in response to the operation code [read request], the memory device outputs a first portion of data synchronously with respect to a rising edge transition of an external clock signal and a second portion of data synchronously with respect to a falling edge transition of the external clock signal [onto a bus]; and

input receiver circuitry to sample the first portion of data and the second portion of data output by the memory device [from the bus synchronously with respect to a rising edge transition of the external clock signal and a second portion of data from the bus synchronously with respect to a falling edge transition of the external clock signal].

158. The controller device of claim 157 wherein the input receiver circuitry includes first latch circuitry to latch the first portion of data, and second latch circuitry to latch the second portion of data.

159. (Amended) The controller device of claim 157 further including a delay lock loop circuit, coupled to the external clock signal, [the delay lock loop circuit generating] to generate a first internal clock signal, wherein the input receiver circuitry samples the first portion of data in response to the first internal clock signal.

160. (Amended) The controller device of claim 159 wherein the delay lock loop circuit generates a second internal clock signal that is complementary to the first internal clock signal, wherein the input receiver circuitry samples the second portion of data in response to the second internal clock signal.

161. The controller device of claim 157 wherein both the rising and falling edge transitions of the external clock signal include voltage swings of less than one volt.

162. (Amended) The controller device of claim 157 wherein the input receiver circuitry samples an amount of data output by the memory device in response to the operation code wherein the amount of data is sampled during a plurality of clock cycles of the external clock signal.

163. (Amended) The controller device of claim 162 wherein the output driver circuitry provides block size information to the memory device, wherein the block size information is representative of the

amount of data output by the memory device in response to the operation code, and wherein, in response to the operation code, the memory device outputs the amount of data during a plurality of clock cycles of the external clock signal [to output in response to a read request to the memory device].

164. (Amended) The controller device of claim 163 wherein the operation code [read request] and the block size information [representative of the amount of data to output] are included in a [read] request packet.

165. (Amended) A method of operation of a memory controller device, the method comprises [comprising]:

issuing an operation code [a write request] to a memory device[,] synchronously with respect to an external clock signal, wherein the operation code instructs the memory device to input first and second portions of data [in response to the write request, the memory device inputs first and second portions of data];

outputting the first portion of data synchronously with respect to a rising [first] edge transition of [an] the external clock signal; and

outputting the second portion of data [from the bus] synchronously with respect to a falling [second] edge transition of the external clock signal.

166. The method of claim 165 wherein the controller device outputs the first portion of data after a delay time transpires.

167. (Amended) The method of claim 165 further including providing to the memory device[access time] information that represents an amount of time which lapses before data is input by [to] the memory device.

168. (Amended) The method of claim 167 wherein the [access time] information is provided in the form of a value and wherein the value is representative of a number of clock cycles of the external clock signal [to transpire before the first portion of the amount of data is available on a bus].

169. The method of claim 165 wherein the first and second edge transitions of the external clock signal include voltage swings of less than one volt.

170. The method of claim 165 wherein the first portion of data and second portion of data include voltage swings of less than one volt.

171. (Amended) The method of claim 165 further including providing address information to the memory device synchronously with respect to [wherein the data is output during a plurality of first and second edge transitions of] the external clock signal.

172. (Amended) The method of claim 165 further including providing block size information to the memory device, wherein the

block size information is representative of an amount of data to be input by the memory device in response to the operation code [in response to a write request].

173. (Amended) The method of claim 172 further including outputting the amount of data to the memory device during a plurality of clock cycles of the external clock signal [which corresponds to the block size information].

174. (Amended) The method of claim 173 further including providing address information to the memory device synchronously with respect to the rising and falling edges of the external clock signal [wherein the data corresponding to the block size information is output during a plurality of first and second edge transitions of the external clock signal].

175. (Amended) The method of claim 174 wherein the block size information, the address information and the operation code are included in a write request packet [165 wherein the first edge transition of the external clock signal is a rising edge transition of the external clock signal, and the second edge transition of the external clock signal is a falling edge transition of the external clock signal].

176. (New) The method of claim 151 further including providing address information to the memory device synchronously with respect to the external clock signal.

177. (New) The method of claim 176 wherein the address information is provided synchronously with respect to rising and falling edges of the external clock signal.

178. (New) The method of claim 176 wherein the address information and the first operation code are provided in a request packet.

179. (New) The method of claim 178 wherein the address information and the first operation code are provided in the same request packet.

180. (New) The method of claim 176 wherein the address information and the first operation code are output onto an external bus, wherein the external bus includes a set of signal lines to multiplex data, control information, and address information.

181. (New) The method of claim 151 wherein the rising edge transition of the external clock signal and the falling edge transition of the external clock signal transpire in the same clock cycle of the external clock signal.

182. (New) The method of claim 151 wherein the first operation code is issued synchronously with respect to the external clock signal.

183. (New) The method of claim 182 wherein the first operation code is output onto an external bus.

184. (New) The method of claim 183 wherein the external bus includes a set of signal lines to multiplex data, control information, and address information.

185. (New) The method of claim 154 wherein the access time information is representative of a number of clock cycles of the external clock signal to transpire before the second portion of data is output by the memory device.

186. (New) The method of claim 151 wherein the first operation code includes precharge information.

187. (New) The controller device of claim 157 wherein the input receiver circuitry samples the first portion of data from an external bus.

188. (New) The controller device of claim 187 wherein the external bus includes a set of signal lines to transmit multiplexed address information, data and control information.

189. (New) The controller device of claim 157 wherein the output driver circuitry and the input receiver circuitry are connected to a common pad.

190. (New) The controller device of claim 157 wherein the output driver circuitry provides the operation code synchronously with respect to the external clock signal.